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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,175	04/27/2001	Warren M. Farnworth	MI22-1703	4157

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EXAMINER	
NGUYEN, VINH P	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,175	FARNWORTH ET AL.	
	Examiner	Art Unit	
	VINH P. NGUYEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-42,54,56-65,67-70,75-89 and 92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-42,54,56-65,67-70,75-89 and 92* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 31-34,35-36,38,40-41,54,56-59,61-65,67-70,75-76,79-80,89 and 92 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano (Japanese Reference # Hei 3-69131).

As to claim 31, Nakano disclose in figures 2b a removable electrical interconnect apparatus for removably engaging electrically conductive pads on a semiconductor substrate (24) having integrated circuitry fabricated therein having an apparatus substrate (10) made of semiconductor material (Silicon), an engagement probe (22) projecting from the apparatus substrate (10) to engage a single conductive pad (25) on a semiconductor substrate (24) having integrated circuitry formed in the semiconductor substrate, the engagement probe comprising semiconductor material (same semiconductor material of the substrate (10)) and having an outer surface comprising an apex in the form of a knife edge line. It appears that the engagement probe of Nakano is inherently configured to removably penetrate a single conductive pad of the semiconductor substrate comprising integrated circuitry and to removably penetrate another signal conductive pad of another semiconductor substrate also comprising integrated circuitry. Furthermore, it is noted that the limitation of "configured to removably penetrate a single conductive pad of the semiconductor substrate comprising integrated circuitry and to removabley penetrate another single conductive pad of another semiconductor substrate also comprising integrated circuitry" is considered as intended use and this limitation does no affect the claimed structure of the instant interconnect apparatus.

As to claim 32, theNakano disclose a projection (21) from the apparatus substrate and wherein the engagement probe (22) is formed on the projection (21).

As to claim 33, the knife edge line projects from a penetration stop plane (horizontal bottom plane of the projection "21").

As to claim 34, Nakano shows the knife edge line (edge and tip of the probe (22)) projects from a penetration stop plane and the knife edge line having a tip and a base at the penetration stop plane).

As to claim 35, Nakano disclose a projection (21) from the apparatus substrate and wherein the engagement probe (22) is formed on the projection (21) and the knife edge line projects from a penetration stop plane (horizontal bottom plane of the projection "21").

As to claims 36,57,59 and 92, it appears that the tip (22) being a distance from the penetration stop plane of about one half the thickness of the single conductive pad.

As to claim 38, Nakano disclose the probe made of the same material (Silicon) as the substrate (10), therefore this semiconductor is considered as "bulk semiconductor substrate".

As to claim 40, the outer surface includes plural knife edge lines configured to engage single contact pads (25).

As to claim 41, wherein the engagement probe of Nakano is formed from a semiconductor substrate (10) and the outer surface includes plural knife edge lines configured to engage single contact pads (25).

As to claim 54,Nakano discloses in figures 2b a removable electrical interconnect apparatus for removably engaging electrically conductive pads on a semiconductor substrate (24) having integrated circuitry fabricated therein having an apparatus substrate (10) made of semiconductor material (Silicon), an engagement probe (22) projecting from the apparatus substrate (10) to engage a single conductive pad (25) on a semiconductor substrate (24) having integrated circuitry formed in the semiconductor substrate, the engagement probe comprising semiconductor material (same semiconductor material of the substrate (10)) and having an outer surface comprising an apex in the form of a knife edge line and wherein the knife edge line is formed on a projection (21) from a substrate (10).

As to claim 56, it appears that the outer surface of Nakano comprises a plurality of apexes as shown in figure 1 having tips (22) and bases (bottom surface of the tip "22") and the penetration stop plane is intermediate the bases and substantially parallel to a surface of the substrate (10).

As to claim 58, Nakano discloses a projection (21) from the apparatus substrate and wherein the engagement probe (22) is formed on the projection (21) and the knife edge line projects from a penetration stop plane (horizontal bottom plane of the projection "21").

As to claim 61, Nakano discloses the probe made of the same material (Silicon) as the substrate (10), therefore this semiconductor is considered as "bulk semiconductor substrate".

As to claim 62, Nakano teaches that the knife edge line is sized and positioned to extend

elevationally above an uppermost surface of the apparatus substrate (10).

As to claim 63, the projection (21) of Nakano includes a surface substantially parallel to a surface of the substrate (10).

As to claim 64, the knife edge line projects elevationally above an upper most surface of the projection (21) which defines the penetration stop plane ((horizontal bottom plane of the projection "21").

As to claim 65, the projection (21) has a surface substantially parallel to a surface of the substrate (10) and the surface of the projection defines the penetration stop plane.

As to claim 67, Nakano discloses the substrate (10) made of the same material (Silicon) therefore this semiconductor is considered as "bulk semiconductor substrate".

As to claims 68-70, Nakano discloses the probe made of the same material (Silicon) as the substrate (10), therefore this semiconductor is considered as "bulk semiconductor substrate".

As t o claims 75-76, the apex (22) of Nakano comprises a solid mass of material devoid of any void space.

As to claim 79, Nakano discloses in figures 2b a removable electrical interconnect apparatus for removably engaging electrically conductive pads on a semiconductor substrate (24) having integrated circuitry fabricated therein having an apparatus substrate (10) made of semiconductor material (Silicon), an engagement probe (22) projecting from the apparatus substrate (10) to engage a single conductive pad (25) on a semiconductor substrate (24) having

integrated circuitry formed in the semiconductor substrate, the engagement probe comprising semiconductor material (same semiconductor material of the substrate (10)) and having an outer surface comprising an apex in the form of a knife edge line and wherein the knife edge line is formed on a projection (21) from a substrate (10) and wherein the knife edge line projects from a penetration stop plane (horizontal bottom plane of the projection "21").

As to claim 80, the apex (tip of the probe "22") of Nakano is configured to penetrate the single conductive pad.

As to claim 89, Nakano discloses in figures 2b a removable electrical interconnect apparatus for removably engaging electrically conductive pads on a semiconductor substrate (24) having integrated circuitry fabricated therein having an apparatus substrate (10) made of semiconductor material (Silicon), an engagement probe (22) projecting from the apparatus substrate (10) to engage a single conductive pad (25) on a semiconductor substrate (24) having integrated circuitry formed in the semiconductor substrate, the engagement probe comprising semiconductor material (same semiconductor material of the substrate (10)) and having an outer surface comprising an apex in the form of a knife edge line and wherein the knife edge line is formed on a projection (21) from a substrate (10) and wherein the knife edge line projects from a penetration stop plane (horizontal bottom plane of the projection "21"). It is noted that the apparatus of Nakano comprises a plurality of apexes (knife edge line) having respective tips and bases and the penetration stop plane (horizontal bottom plane of the projection "21") is

intermediate the bases and substantially parallel to a surface of a substrate (10).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 37,39,42,60,77-78 and 81-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (Japanese Reference # Hei 3-69131) in view of Blonder et al (Pat # 4,937,653).

As to claims 37 and 60, Nakano discloses a remobvable electrical interconnect as mentioned in previous paragraph. However, Nakano does not teach that the outermost portions of the apex (the knife edge line) comprises a first electrically conductive material and the conductive pads for which the apparatus is adapted to engage have outermost portions comprising a second electrically conductive material wherein the first and second electrically conductive materials being different.

Blonder et al teach that outermost portions of the apex comprise a first electrically conductive material (gold-plated nickel', col 7, In 64-66), and wherein the conductive pads for which the apparatus is adapted to 'engage have outermost portion comprising a second electrically conductive material (gold pads); the first and second electrically conductive materials being different (col 5, lines 57-61 and col 7, lines 63- col. 8, line 6).

It would have been obvious for one of ordinary skill in the art to provide the teaching of coating the apex with a first conductive material as taught by Blonder et al in order to protect the apex (knife edge line) from damage during the test.

As to claim 39, Blonder et al disclose the knife-edge Iine includes an outer conductive Iayer (gold-plated nickel noted at col 7, In 63 - col 8, In 6)).

As to claim 42, discloses a remobvable electrical interconnect as mentioned in previous paragraph. However, Nakano does not teach that the knife edge lines include outer conductive layers.

Blonder et al teach that the knife edge lines include outer conductive layers (gold-plated nickel', col 7, In 64-66),

It would have been obvious for one of ordinary skill in the art to provide the teaching of coating the knife edge lines with outer conductive layers as taught by Blonder et al in order to protect the knife edge lines from damage during the test.

As to claims 77-78, Nakano discloses in figures 2b a removable electrical interconnect apparatus for removably engaging electrically conductive pads on a semiconductor substrate (24) having integrated circuitry fabricated therein having an apparatus substrate (10) made of semiconductor material (Silicon), an engagement probe (22) projecting from the apparatus substrate (10) to engage a single conductive pad (25) on a semiconductor substrate (24) having

integrated circuitry formed in the semiconductor substrate, the engagement probe comprising semiconductor material (same semiconductor material of the substrate (10)) and having an outer surface comprising an apex in the form of a knife edge line. Nakano does not disclose a second semiconductor substrate with a second electrically conductive pad and integrated circuitry formed using the second semiconductor substrate. However, by having a second semiconductor would have been considered as duplication of part and it would be considered as obvious design choice since it does not effect the operation of the instant claimed apparatus. (see *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)). Furthermore, it appears that the engagement probe of Nakano is inherently configured to removably engage the first electrically conductive pad and to removably engage the second electrically conductive pad. Furthermore, it is noted that the limitation of "configured to removably engage the first electrically conductive pad and to removably engage the second electrically conductive pad is considered as intended use and this limitation does no affect the claimed structure of the instant interconnect apparatus.

As to claims 81-88, Nakano discloses a remobvable electrical interconnect as mentioned in previous paragraph. However, Nakano does not teach that the knife edge line comprises a triangular prism or a polyhedron. However, the shape and size of the knife edge line would have been an obvious design choice sine the criticality of these features have not been established by Applicants. (see *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966)).

5. Applicant's arguments with respect to claims 31-42,54,56-65,67-70,75-89,92 filed on 08/10/06 have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HA T. NGUYEN can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VINH P NGUYEN
Primary Examiner
Art Unit 2829
11/09/06